## REMARKS

Applicants thank the Examiner for the very thorough consideration given the present application.

Claims 1, 3-5, 8-10, 12 and 13 are now present in this application. By this reply, claim 1, 5 and 10 have been amended, and claims 3, 4, 8, 9, 12 and 13 are canceled. Accordingly, claims 1, 5 and 10 are currently pending.

*Rejections under 35 U.S.C. §103*

Claims 1, 3-5, 8-10, 12 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen (US 5,648,793) in view of Yamazaki (US 6,522,319) and Wada et al. (JP 01-106,017) and further in view of Asada et al. (US 5,867,141).

Applicant respectfully traverses this rejection on grounds that the applied references, whether taken singly or combined, fail to teach or suggest the combination of features recited by the amended independent claims 1, 5 and 10.

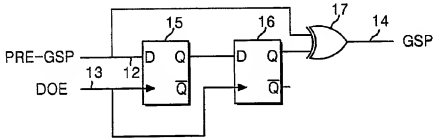
Independent claim 1 recites a method of driving a liquid crystal display panel of dot inversion system including, in part, "a first input line supplied with a pre-gate start pulse and a second input line supplied with a data output enable signal (DOE) for controlling data output of a data driving integrated circuit, wherein the data driving integrated circuit applies data to the data lines in response to the data output enable signal, and wherein the data output enable signal is ***directly*** applied to the data driving integrated circuit and the pre-charging controller; … first delay means for delaying the pre-gate start pulse from the first input line by one clock interval of the data output enable signal in response to the data output enable signal; second delay means for delaying the delayed pre-gate start pulse from the first delay means by one clock interval of the data output enable signal in response to the data output enable signal; … wherein polarity inversion of the data signals applied to the liquid crystal cells connected to

the first and second gate lines is made in at least two clock time intervals **prior to an application of the active data signal**; wherein gate and data control signals for applying data to the liquid crystal cells connected to the first and second gate lines are applied in at least two clock time intervals **before the gate and data control signals become effective data**". *(Emphasis added)*

Similarly, independent claim 5, as amended, recites a driving apparatus for liquid crystal display panel of dot inversion including, in part, "a data driving integrated circuit supplying data to the data lines of the liquid crystal display panel in response to a data output enable signal (DOE), and wherein the data output enable signal is ***directly*** applied to the data driving integrated circuit and the pre-charging controller; … first delay means for delaying the pre-gate start pulse from the first input line by one clock interval of the data output enable signal in response to the data output enable signal; second delay means for delaying the delayed pre-gate start pulse from the first delay means by one clock interval of the data output enable signal in response to a data output enable signal; … wherein polarity inversion of the data signals applied to the liquid crystal cells connected to the first and second gate lines is made in at least two clock time intervals **prior to an application of the active data signal**; wherein gate and data control signals for applying data to the liquid crystal cells connected to the first and second gate lines are applied in at least two clock time intervals **before the gate and data control signals become effective data**". *(Emphasis added)*

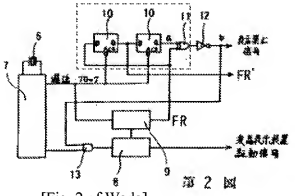
Similarly, independent claim 10, as amended, recites a device for driving a liquid crystal display panel including, in part, "a data driving integrated circuit supplying data to the data lines in response to a data output enable signal (DOE), and wherein the data output enable signal is ***directly*** applied to the data driving integrated circuit and the pre-charging

controller; ... first delay means for delaying the pre-gate start pulse from the first input line by one clock interval of the data output enable signal in response to the data output enable signal; second delay means for delaying the delayed pre-gate start pulse from the first delay means by one clock interval of the data output enable signal in response to a data output enable signal; ... wherein polarity inversion of the data signals applied to the liquid crystal cells connected to the first and second gate lines is made in at least two clock time intervals **prior to an application of the active data signal**; wherein gate and data control signals for applying data to the liquid crystal cells connected to the first and second gate lines are applied in at least two clock time intervals **before the gate and data control signals become effective data**". *(Emphasis added)*




[Fig. 7 of claimed invention]

As shown in Fig. 7 of the claimed invention, the first delay means 15 are provide with the Data Output Enable signal (DOE) which is used to make the data driving circuit apply the data to the data lines. That is to say, the data driving circuit applies the data to the data lines in response to the data output enable signal. Similarly, the second delay means 16 are provided with the data output enable signal.

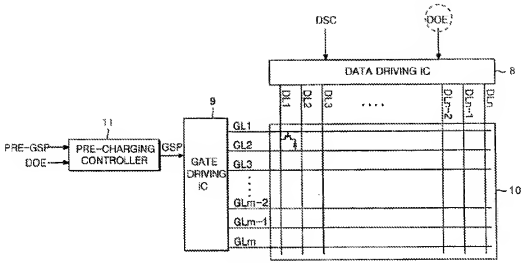



[Fig. 2 of Wada]

In contrast to the claimed invention, Wada's flip-flops 10 are provided with a delayed clock signal 70-7 from the frequency dividing circuit 7. That is to say, Wada fails to teach or suggest the features of the data output enable signal DOE supplied to the first delay means 15 and second delay means 16. That is to say, the reference Wada is completely silent about the claimed feature of the data output enable signal which is used to make the data driving circuit apply the data to the data lines.

Accordingly, the data output enable signal used to make the data driving circuit apply the data to the data lines is totally different from the delayed clock signal from the frequency dividing circuit 7.

Thanks to the features of the claimed invention, both the firs and second delay means 15, 16 are able to be driven by the data output enable signal DOE without additional signals.




[Fig. 6 of claimed invention]

Moreover, the data output enable signal DOE is ***directly applied*** to the data driving IC 8 and the pre-charging controller 11 as shown in the above Fig. 6. Therefore, the data output enable signal ***directly affects*** the data driving IC in the operation of applying the data to the data lines.

However, the delayed clock signal 70-7 of Wada is ***NOT directly*** supplied to the data driving integrated circuit (element 4 of Fig. 1) as shown in Figs. 1 and 4 of Wada. Therefore, it is obvious that the delayed clock signal DOES NOT affect the data driving IC directly.

Accordingly, the data output enable signal directly applied to the data driving circuit to directly affects the data driving IC in the operation of applying the data to the data lines is totally different from the delayed signal from the frequency dividing circuit 7.

In addition, Chen does not disclose the claimed invention's features of "polarity inversion of the data signals applied to the liquid crystal cells connected to the first and second gate lines is made in at least two clock time intervals **prior to an application of the**

**active data signal**" and "gate and data control signals for applying data to the liquid crystal cells connected to the first and second gate lines are applied in at least two clock time intervals **before the gate and data control signals become effective data**"

## CONCLUSION

In view of the foregoing amendments and remarks, Applicant respectfully requests the reconsideration and the timely allowance of the pending claims. Should the Examiner believe that there are any issues outstanding after consideration of this response, the Examiner is invited to contact Applicant's undersigned representative to expedite prosecution.

If there are any other fees due in connection with the filing of this response, please charge the fees to our Deposit Account No. 50-0310. If a fee is required for an extension of time under 37 C.F.R. § 1.136 not accounted for above, such an extension is requested and the fee should also be charged to our Deposit Account.

Respectfully submitted,

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